OIPE 65798 AUG 30 2004 PATENT & TRADEMARK OFFICE

US005811318A

United States Patent [19]

Kwcon

[11] Patent Number: 5,811,318

[45] Date of Patent: Sep. 22, 1998

[54] METHOD FOR MANUFACTURING A LIQUID CRYSTAL DISPLAY

[75] Inventor: Young-chan Kwcon, Seoul, Rep. of Korea

[73] Assignee: Samsung Electronics Co., Ltd., Suwon, Rep. of Korea

[21] Appl. No.: 770,796

[22] Filed: Dec. 20, 1996

[30] Foreign Application Priority Data

Dec. 28, 1995 [KR] Rep. of Korea 95-62170
May 29, 1996 [KR] Rep. of Korea 96-18516

[51] Int. Cl.[6] H01L 21/84

[52] U.S. Cl. 438/30; 438/158; 257/59; 349/152

[58] Field of Search 438/30, 158, 159, 438/160, 592, 182, 200; 257/59, 72; 349/46, 139, 152, 149

[56] References Cited

U.S. PATENT DOCUMENTS

5,075,244	12/1991	Sakai et al.	437/41
5,177,577	1/1993	Taniguchi et al.	257/59
5,187,604	2/1993	Taniguchi et al.	359/88
5,359,206	10/1994	Yamamoto et al.	257/59
5,555,112	9/1996	Oritsuki et al.	359/59
5,668,379	9/1997	Ono et al.	257/59

FOREIGN PATENT DOCUMENTS

5-152573 6/1993 Japan .

6-188419 7/1994 Japan .

Primary Examiner—Charles L. Bowers, Jr.
Assistant Examiner—Laura Schillinger
Attorney, Agent, or Firm—Jones & Volentine, L.L.P.

[57] ABSTRACT

A method for manufacturing a liquid crystal display which reduces the number of photolithography processes is provided. The method includes the steps of forming a gate electrode and a gate pad by depositing a first metal film and a second metal film on a substrate of a TFT area and a gate-pad connecting area, respectively, in the described order, by a first photolithography process, forming an insulating film on the entire surface of the substrate on which the gate electrode and the gate pad are formed, forming a semiconductor film pattern on the insulating film of the TFT area by a second photolithography process, forming a source electrode/drain electrode and pad electrode composed of a third metal film using a third photolithography process in the TFT portion and pad portion, respectively, forming a passivation film pattern which exposes a portion of the drain electrode, a portion of the gate pad, and a portion of the pad electrode by a fourth photolithography process, exposing the first metal film by etching the second metal film which constitutes the gate pad using the passivation film pattern as a mask, and forming a pixel electrode connected to the drain electrode of the TFT area for connecting the gate pad of the gate-pad connecting area to the pad electrode of the pad area using a fifth photolithography process. Therefore, it is possible to reduce the number of photolithography processes, to improve the manufacturing yield, and to suppress growth of a hillock of an Al film.

15 Claims, 8 Drawing Sheets